AMENDMENTS IN THE CLAIMS:

1-26. (Canceled)

27. (Previously Presented) A frequency control apparatus, comprising:

a signal input section for inputting a reproduction signal from a recording medium, wherein a recording symbol is encoded by (1, 7) RLL modulation system and a synchronization pattern includes 2T9T9T when a standard cycle of a symbol length of the recording symbol is defined as T;

an analog/digital conversion section for converting the reproduction signal into a multiple bit digital signal based on a clock signal;

a low noise suppression section for suppressing low noise component included in the multiple bit digital signal;

a maximum likelihood decoding section for performing a maximum likelihood decoding on the multiple bit digital signal having the suppressed low noise component in accordance with a state transition rule along the (1, 7) RLL modulation system and converting the multiple bit digital signal into a binary signal;

a maximum pattern length detection section for detecting a maximum pattern length during a predetermined period from the binary signal converted by the maximum likelihood decoding section;

a minimum pattern length detection section for detecting a minimum pattern length during the predetermined period from the multiple bit digital signal having the suppressed low noise component;

a cycle information determination section for selecting the maximum pattern length or the minimum pattern length that is considered optimum as cycle information from the detected maximum pattern length and minimum pattern length based on a comparison result of the detected maximum pattern length and minimum pattern length;

a frequency error detection section for determining a frequency error amount based on a difference between the maximum pattern length or the minimum pattern length detected when a cycle of the clock signal is the standard cycle T and the cycle information; and

a clock oscillation section for adjusting the frequency of the clock signal based on the determined frequency error amount and outputting the adjusted clock signal.

28. (Previously Presented) A frequency control method, comprising the steps of:

inputting a reproduction signal from a recording medium, wherein a recording symbol is encoded by (1, 7) RLL modulation system and a synchronization pattern includes 2T9T9T when a standard cycle of a symbol length of the recording symbol is defined as T;

converting the reproduction signal into a multiple bit digital signal based on a clock signal;

suppressing low noise component included in the multiple bit digital signal;

performing a maximum likelihood decoding on the multiple bit digital signal having the suppressed low noise component in accordance with a state transition rule along the (1, 7) RLL modulation system and converting the multiple bit digital signal into a binary signal;

detecting a maximum pattern length during a predetermined period from the binary signal converted by the maximum likelihood decoding section;

detecting a minimum pattern length during the predetermined period from the multiple bit digital signal having the suppressed low noise component;

selecting the maximum pattern length or the minimum pattern length that is considered optimum as cycle information from the detected maximum pattern length and minimum pattern length based on a comparison result of the detected maximum pattern length and minimum pattern length;

determining a frequency error amount based on a difference between the maximum pattern length or the minimum pattern length detected when a cycle of the clock signal is the standard cycle T and the cycle information; and

adjusting the frequency of the clock signal based on the determined frequency error amount and outputting the adjusted clock signal.

29. (Currently Amended) A ~~control program for executing on~~ computer readable medium having a program stored thereon, wherein executing the program causes a computer to perform a frequency control method, the method comprising the steps of:

inputting a reproduction signal from a recording medium, wherein a recording symbol is encoded by (1, 7) RLL modulation system and a synchronization pattern includes 2T9T9T when a standard cycle of a symbol length of the recording symbol is defined as T;

converting the reproduction signal into a multiple bit digital signal based on a clock signal;

suppressing low noise component included in the multiple bit digital signal;

performing a maximum likelihood decoding on the multiple bit digital signal having the suppressed low noise component in accordance with a state transition rule along the (1, 7) RLL modulation system and converting the multiple bit digital signal into a binary signal;

detecting a maximum pattern length during a predetermined period from the binary signal converted by the maximum likelihood decoding section;

detecting a minimum pattern length during the predetermined period from the multiple bit digital signal having the suppressed low noise component;

selecting the maximum pattern length or the minimum pattern length that is considered optimum as cycle information from the detected maximum pattern length and minimum pattern length based on a comparison result of the detected maximum pattern length and minimum pattern length;

determining a frequency error amount based on a difference between the maximum pattern length or the minimum pattern length detected when a cycle of the clock signal is the standard cycle T and the cycle information; and

adjusting the frequency of the clock signal based on the determined frequency error amount and outputting the adjusted clock signal.

30. (Previously Presented) An information reproduction apparatus for reproducing information from an information recording medium, the apparatus comprising:

a signal input section for inputting a reproduction signal from a recording medium, wherein a recording symbol is encoded by (1, 7) RLL modulation system and a synchronization pattern includes 2T9T9T when a standard cycle of a symbol length of the recording symbol is defined as T;

an analog/digital conversion section for converting the reproduction signal into a multiple bit digital signal based on a clock signal;

a low noise suppression section for suppressing low noise component included in the multiple bit digital signal;

a maximum likelihood decoding section for performing a maximum likelihood decoding on the multiple bit digital signal having the suppressed low noise component in accordance with a state transition rule along the (1, 7) RLL modulation system and converting the multiple bit digital signal into a binary signal;

a maximum pattern length detection section for detecting a maximum pattern length during a predetermined period from the binary signal converted by the maximum likelihood decoding section;

a minimum pattern length detection section for detecting a minimum pattern length during the predetermined period from the multiple bit digital signal having the suppressed low noise component;

a cycle information determination section for selecting the maximum pattern length or the minimum pattern length that is considered optimum as cycle information from the detected maximum pattern length and minimum pattern length based on a comparison result of the detected maximum pattern length and minimum pattern length;

a frequency error detection section for determining a frequency error amount based on a difference between the maximum pattern length or the minimum pattern length detected when a cycle of the clock signal is the standard cycle T and the cycle information;

a clock oscillation section for adjusting the frequency of the clock signal based on the determined frequency error amount and outputting the adjusted clock signal; and

a reproduction section for reproducing information from the information recording medium based on the adjusted clock signal.

31. (Previously Presented) An information reproducing method for reproducing information from an information recording medium, the method comprising the steps of:

inputting a reproduction signal from a recording medium, wherein a recording symbol is encoded by (1, 7) RLL modulation system and a synchronization pattern includes 2T9T9T when a standard cycle of a symbol length of the recording symbol is defined as T;

converting the reproduction signal into a multiple bit digital signal based on a clock signal;

suppressing low noise component included in the multiple bit digital signal;

performing a maximum likelihood decoding on the multiple bit digital signal having the suppressed low noise component in accordance with a state transition rule along the (1, 7) RLL modulation system and converting the multiple bit digital signal into a binary signal;

detecting a maximum pattern length during a predetermined period from the binary signal converted by the maximum likelihood decoding section;

detecting a minimum pattern length during the predetermined period from the multiple bit digital signal having the suppressed low noise component;

selecting the maximum pattern length or the minimum pattern length that is considered optimum as cycle information from the detected maximum pattern length and minimum pattern length based on a comparison result of the detected maximum pattern length and minimum pattern length;

determining a frequency error amount based on a difference between the maximum pattern length or the minimum pattern length detected when a cycle of the clock signal is the standard cycle T and the cycle information;

adjusting the frequency of the clock signal based on the determined frequency error amount and outputting the adjusted clock signal; and

reproducing information from the information recording medium based on the adjusted clock signal.